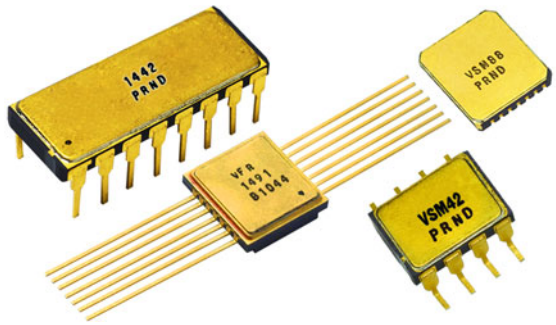
Custom Hermetically Sealed Precision Resistor Network Devices (PRND) With Screen/Test Flow in Compliance with EEE-INST-002 (Tables 2A and 3A, Film/Foil, Level 1) and MIL-PRF-83401



INTRODUCTION

PRND (Precision Resistor Network Devices) are custom made, hermetically sealed networks which incorporate all the performance features of the Bulk Metal® Foil technology. The PRND can be configured to various circuit schematics and specifications the customer requests. Multiple Bulk Metal® Foil hybrid chip resistors are arranged within the devices and connected by gold-wire bonding. Hermetic sealing of Vishay Foil Resistors' networks enhances their already inherently stable environmental performance. The result is improved load life stability and better performance during high temperature and moisture exposure.

The combination of the ceramic package which has the advantage of electrical isolation on the underside and high heat dissipation capability ("heat-sink effect"), together with the hermeticity and the location of the chips within the package help preserve uniform conditions inside it.

The best long term tracking stability for thermally coupled resistors is guaranteed by the mounting of the resistors in the same hermetically sealed package. This assembly ensures uniform environmental conditions for the resistors. The electrical specs in a hermetically sealed network hold their tight TC ratio under the combined influences of temperature, load and time.

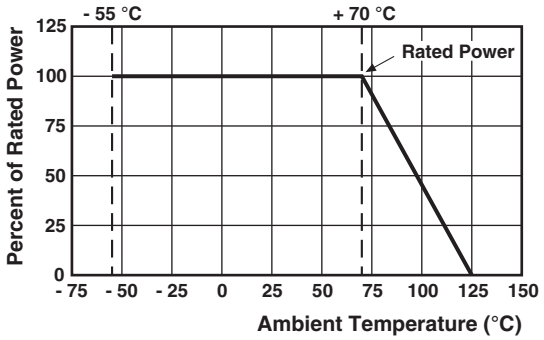
The Bulk Metal® Foil technology's advantage in such a construction assures remarkable performance due to the following factors: fundamentally low TCR, very small drift with load over time, common behavior: all drifts move in the same direction with temperature, load and time, TCR and tolerance match and excellent tracking.

Vishay Foil Resistors' hermetic networks are based on fabrication from a standing inventory of packages and resistor chips. This permits quick delivery of prototypes since there are no masks to design or trial processing to be made. Further, it allows a large combination of values, tolerances and circuits. There are normally no engineering or setup charges, and no minimum quantities are required.

FEATURES

- **Temperature coefficient of resistance (TCR):**
  Absolute: ± 2 ppm/°C typical
  Tracking: ± 2 ppm/°C typical
  (- 55 °C to + 125 °C, + 25 °C ref.)
- Resistance range: 5 Ω to 60 kΩ (1)
- Resistance tolerance match: to ± 0.005 %
- Hermetically sealed for maximum environmental protection
- Power rating: 0.4W to 1.4W per package, at +70 °C
  50 mW to 150 mW per resistor, at +70 °C
- **Load life stability: 0.05% typical (rated power at 70 °C, 2000 h)**
- **Load life stability ratio: 0.02% typical (rated power at 70 °C, 2000 h)**
- **Shelf life stability: ± 2 ppm typical after at least 6 years**
- Vishay Foil resistors are not restricted to standard values; specific "as required" values can be supplied at no extra cost or delivery (e.g. 1K2345 vs. 1K)
- Thermal stabilization time < 1 s (nominal value achieved within 10 ppm of steady state value)
- Rise time: 1 ns effectively no ringing
- Non-inductive, non-capacitive design
- Current noise: 0.010 μV_{RMS}/V of applied voltage (< - 40 dB)
- Voltage coefficient: 0.1 ppm/V
- Non inductive: 0.08 µH
- Non hot spot design
- Terminal finish: gold plated (lead (Pb)-free)
- For better performances, please contact foil@vishaypg.com

FIGURE 1 - POWER DERATING CURVE (2)



Notes

(1) For internal configuration and circuit schematic, please contact Application Engineering

(2) For power rating per each package, please refer to page 5

TABLE 1 - PRND NETWORK PERFORMANCE VERSUS MIL-PRF-83401 SPEC PERFORMANCE			
TEST OR CONDITION		**MIL-PRF-83401**	**VISHAY FOIL RESISTORS**
		C	**Typical**
Resistance Temp Characteristic	**ppm/°C**	± 50	±2
Tracking To Reference Element (- 55 to + 125 °C)	**ppm/°C**	± 5	±2
Max Ambient Temp at Rated Wattage		+ 70 °C	
Max Ambient Temp at Zero Power		+ 125 °C	
Thermal Shock and Power Conditioning		± 0.25 % ± 0.03 %	±0.015% ±0.015%
Low Temperature Operation	**ΔR** **ΔRatio**	± 0.10 % ± 0.02 %	±0.01% ±0.01%
Short Time Overload	**ΔR** **ΔRatio**	± 0.10 % ± 0.02 %	±0.01% ±0.01%
Terminal Strength	**ΔR** **ΔRatio**	± 0.10 % ± 0.03 %	±0.01% ±0.01%
Resistance to Soldering Heat	**ΔR** **ΔRatio**	± 0.10 % ± 0.02 %	±0.01% ±0.01%
Moisture Resistance	**ΔR** **ΔRatio**	± 0.20 % ± 0.02 %	±0.01% ±0.01%
Shock (Specified Pulse)	**ΔR** **ΔRatio**	± 0.25 % ± 0.03 %	±0.01% ±0.01%
Vibration, High Frequency	**ΔR** **ΔRatio**	± 0.25 % ± 0.03 %	±0.01% ±0.01%
Load Life (Per EEE-INST-002) **(+ 70 °C, Full Power, 2000 hours)**	**ΔR** **ΔRatio**	± 0.10 % ± 0.03 %	±0.05 % ±0.02%
+ 25 °C Power Rating **(1000 hrs.)**	**ΔR** **ΔRatio**	± 0.10 % ± 0.03 %	±0.01% ±0.01%
High Temperature Exposure **(+ 125 °C, 100 hours)**	**ΔR** **ΔRatio**	± 0.10 % ± 0.03 %	±0.01% ±0.01%
Low Temperature Storage	**ΔR** **ΔRatio**	± 0.10 % ± 0.02 %	±0.01% ±0.01%
Insulation Resistance		10,000 MΩ	
Resistance Tolerance and, **when applicable,** **Resistance Ratio Accuracy**		± 0.1 %(B) ± 0.5 %(D) ± 1.0 %(F)	±0.1%(B) ±0.5%(D)

NOTE:
1. ΔR's are not cumulative. For purposes of determining reliability calculations, consider the characteristics shown as figures of merit and allow no more than ± 0.05 ΔR lifetime. Allow proportionately less if the severity of anticipated environmental stress is small compared to the tests as defined in MIL-PRF-83401.

TABLE 2 - EEE-INST-002 (table 2A Film/Foil, level 1) **100 % TESTS/INSPECTIONS**[1][2]	
RC Record	In tolerance
Thermal Shock	25 x (- 65 °C to + 125 °C)
Power Conditioning	+ 25 °C, 100 h, 1.5 rated power (per each chip, not to exceed max working voltage)
RC Record (Final)	In tolerance. ΔR= 0.03%; ΔR Ratio = 0.03%
Hermetic Seal	1. Fine Leak: < $5x10^{-7}$ cc/sec 2. Gross Leak: No bubbles (MIL-STD-202 - Method 112, Test condition .D)
Visual Inspection	Magnification x 30 to x 60
Final Inspection	5 % PDA on combination of: final tolerance, ΔR and ΔR Ratio over Thermal Shock + Power conditioning and Hermetic Seal
Mechanical Inspection	Dimensions, workmanship, 3 units sample size

Notes

(1) Measurement error allowed for DR limits: 0.01 Ω.

(2) For prototype units, append a "U" to the model number. These units have all of the table 2A 100 % tests performed, with no destructive qualification testing required.

TABLE 3 - EEE-INST-002 (table 3A Film/Foil, level 1) **DESTRUCTIVE TESTS - MIL-PRF-83401-** Typical Limits[4][5][6]		
Group 2	Sample size: 3(0)	
	Solderability	MIL-STD-202, method 208
	Resistance to solvents	MIL-STD-202, method 215
Group 3	Sample size: 10(0) - mounted on PCB	
	TCR measurement per MIL-STD-202, method 304 - 55 °C/+ 25 °C/+ 125 °C (available also per customer's unique specifications)	
	Low temperature storage per MIL-PRF-83401	- 65 °C ± 2 °C, 24 h ± 4 h ambient no load dwell for 2 h to 8 h at + 25 °C
	Low temperature operation per MIL-PRF-83401	- 65 °C ambient no load dwell for 1 h rated power for 45 min no load dwell at + 25 °C for 24 h ± 4 h
	Short time overload per MIL-STD-83401	6.25 x rated power at + 25 °C for 5 s, not to exceed maximum working voltage
	Terminal strength per MIL STD 202 method 211 Conditions A and C	Applied Force to specification
	Hermetic Seal (MIL-STD-202 - Method 112, Test condition .D)	1. Fine Leak: < $5x10^{-7}$ cc/s 2. Gross Leak: No bubbles
Group 4	Sample size: 9(0) - mounted on PCB	
	Dielectric Withstanding Voltage (DWV)	200V RMS, 1min
	Insulation Resistance (IR) 100V	>10^4MΩ
	Resistance to soldering heat	10 s at + 260 °C reflow method
	Moisture resistance per MIL-STD-202, method 106 (Including DWV and IR)	240 h, no power
	Hermetic Seal (MIL-STD-202 - Method 112, Test condition D)	1. Fine Leak: < $5x10^{-7}$ cc/s 2. Gross Leak: No bubbles
	Visual Inspection	
Group 5	Sample size: 9(0)	
	Shock per MIL-STD-202, method 213, condition I	100G, 6 ms axes X, Y, Z, 3 shocks per axis
	Vibration per MIL-STD-202, method 204, condition D	10 Hz to 2000 Hz, 20G, X, Y, Z axes, 4 h per axis
	Hermetic Seal (MIL-STD-202 - Method 112, Test condition .D)	1. Fine Leak: < $5x10^{-7}$ cc/s 2. Gross Leak: No bubbles
Group 6	Sample size: 12(0) - mounted on PCB	
	Life test per MIL-PRF-83401	2000 h, + 70 °C, rated power

TABLE 3 - EEE-INST-002 (table 3A Film/Foil, level 1) DESTRUCTIVE TESTS - MIL-PRF-83401- Typical Limits[4][5][6]		
Group 7B[7]	Sample Size: 8(1)	
	Adhesion per MIL-PRF-914	50gr, 30 sec
Group 9	Sample size: 5(0)	
	High temperature exposure per MIL-PRF-83401	100 h, + 125 °C, no power
	Dielectric Withstanding Voltage (DWV)	200V RMS, 1min
	Insulation Resistance (IR) 100V	$>10^4 M\Omega$

Notes

(4) ΔRatio refers to the change in ratio between resistors within the network package from before, to after, the specified test.

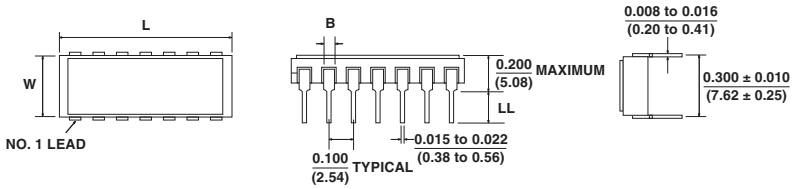
(5) Units selected randomly from lots which successfully passed the table 2A.

(6) Measurement error allowed for ΔR limits: 0.01 Ω.

(7) Applicable only to LCC packages.

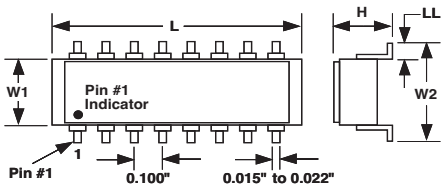
PACKAGE SIZES AND CHARACTERISTICS[1][2]

FIGURE 2 - DUAL-IN-LINE PACKAGE (DIP) CONFIGURATION



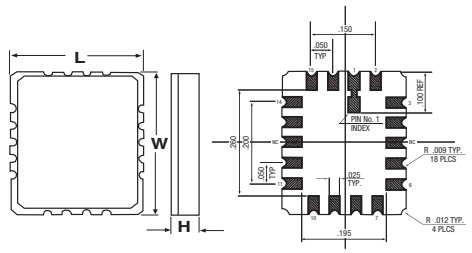
MODEL	NO. OF PINS	MAXIMUM DIMENSIONS IN INCHES (MM)				CHIP CAPACITY		MAXIMUM POWER RATING (WATTS) AT + 70 °C
		L	W	B	LL (Typical)	V5X5	V15X5	
1442	8	0.520 ± 0.020 (13.21 ± 0.51)	0.310 ± 0.010 (7.874± 0.025)	0.054 (1.37)	0.170 (4.318)	**12**	**4**	0.4
1445	14	0.770 ± 0.008 (19.558±0.203)	0.310± 0.08 (7.874± 2.032)	0.047 (1.194)	0.170 (4.318)	**30**	**10**	1.2
1446	16	0.800 ± 0.010 (20.32±0.254)	0.310 ± 0.010 (7.874± 0.025)	0.049 (1.245)	0.170 (4.318)	**36**	**12**	1.4

FIGURE 3 - GULL WING CONFIGURATION



MODEL	NO. OF PINS	MAXIMUM DIMENSIONS IN INCHES (MM)					CHIP CAPACITY		MAXIMUM POWER RATING (WATTS) AT + 70 °C
		L	W1	W2	H	LL	V5X5	V15X5	
VSM42	8	0.520 ± 0.020 (13.21 ± 0.51)	0.310 ± 0.010 (7.874± 0.025)	0.440 ± 0.030 (11.176 ± 0.762)	0.180 (4.572)	0.075 ± 0.015 (1.905 ± 0.381)	12	4	0.4
VSM45	14	0.770 ± 0.008 (19.558±0.203)	0.310± 0.08 (7.874± 2.032)	0.440 ± 0.030 (11.176 ± 0.762)	0.180 (4.572)	0.075 ± 0.015 (1.905 ± 0.381)	30	10	1.2
VSM46	16	0.800 ± 0.010 (20.32±0.254)	0.310 ± 0.010 (7.874± 0.025)	0.450 ± 0.020 (11.43± 0.508)	0.180 (4.572)	0.045 ± 0.010 (1.143 ± 0.254)	36	12	1.4

FIGURE 4 - LEADLESS CHIP CARRIER (LCC) CONFIGURATION



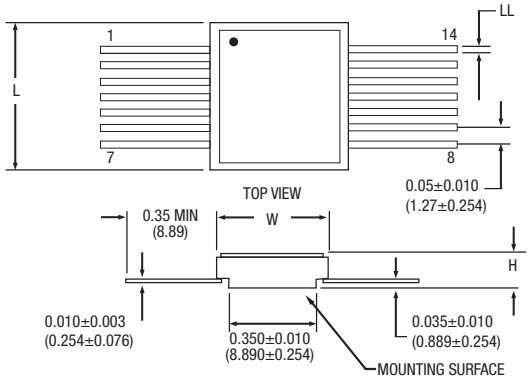
MODEL	NO. OF PINS	MAXIMUM DIMENSIONS IN INCHES (MM)				CHIP CAPACITY		MAXIMUM POWER RATING (WATTS) AT + 70 °C
		L	W	H	LL	V5X5	V15X5	
VSM85	16	0.295 (7.493)	0.360 (9.144)	0.090 (2.286)	N/A	**12**	**4**	0.4

Notes

(1) Other hermetic package configurations also available.

(2) For internal configuration and circuit schematic, please contact Application Engineering.

FIGURE 5 - FLATPACK CONFIGURATION



MODEL	NO. OF PINS	MAXIMUM DIMENSIONS IN INCHES (MM)				CHIP CAPACITY		MAXIMUM POWER RATING (WATTS) AT + 70 °C
		L	W	H	LL	V5X5	V15X5	
1491	14	0.470±0.010 (11.938±0.254)	0.450±0.010 (11.43±0.254)	0.140 Max (3.556)	0.17±0.020 (4.318±0.508)	18	12	1.4

TABLE 4 - MECHANICAL SPECIFICATIONS

Resistive Element	High precision Bulk Metal® Foil chips
Body	Ceramic package: 94 % alumina (Al_2O_3)
Lid	Gold plated kovar
Terminals	Alloy 42 (iron nickel) with 100 µ" gold plating (MIL-STD-1276, type G-21-A)
Internal Connections	Gold wire bonding
Solderability	Per MIL-PRF-83401
Marking Resistance to Solvents	Permanency testing per MIL-PRF-83401

FIGURE 6 - SAMPLE CIRCUIT DESIGN AND CHIP LAYOUT (VSM42 MODEL)

NOTE:

Usable area is represented by the dotted lines - a rectangle 0.150 Inches x 0.200 Inches. Illustrations not to scale. Chips shown undersize for clarity. Drawing view is from the top looking down into the package.

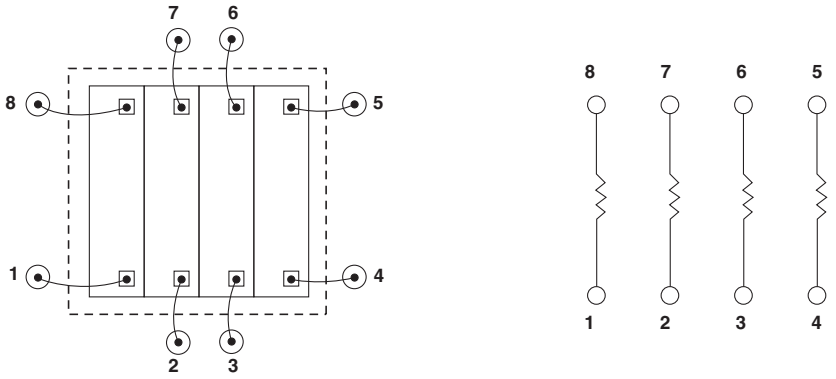
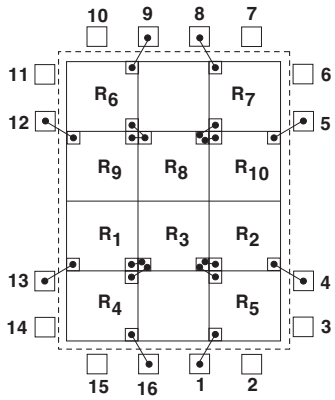
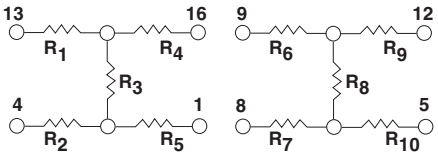


FIGURE 7 - SAMPLE CIRCUIT DESIGN AND CHIP LAYOUT (VSM85 MODEL)



NOTE:

Usable area is represented by the dotted lines - a rectangle 0.150" x 0.200". Illustrations not to scale. Chips shown undersize for clarity. Drawing view is from the top looking down into the package.



ORDERING INFORMATION

Hermetically Sealed Precision Resistor Network Device (PRND) are built to your requirements. Send your schematic and electrical requirements to the Applications Engineering Department (foil@vishaypg.com). A unique part number will be assigned which defines all aspects of your network.

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